

DIRECT CONVERSION FOR FLEX PAGING RECEIVERS — A FEASIBILITY STUDY

Zhiheng CHEN and Jack LAU

Department of Electrical & Electronic Engineering
The HONG KONG University of Science & Technology
Clear Water Bay, Kowloon, HONG KONG

Abstract

To achieve an integrated solution for the 6400 bps FLEX paging receiver, we examined the direct conversion architecture and addressed two major problems that may obstruct the implementation: (1) the compensation of the DC offset, and (2) the design of a 4-level FSK demodulator at zero-IF. Simulation results show that the combination of harmonic mixers with a zero-crossing-interpolation based demodulator is a possible solution.

Introduction

The FLEX protocol has been promoted as a new standard for high speed paging. Its maximum speed of 6400 bps is more than twice that of the 2400 bps offered by the POCSAG used today. In new emerging markets such as China, FLEX is widely being adopted. However, unlike the POCSAG system where direct conversion architectures have been successfully implemented[1], FLEX systems rely heavily on the conventional heterodyne, limiter-discriminator based demodulation scheme. Here we discuss two major issues that contribute to the problem and propose a solution.

The DC Offset Problem and Harmonic Mixing

While the DC offset problem is not of significant concern in POCSAG receivers, it becomes a major issue in the 4-FSK FLEX pagers. Figure 1 shows the analytical power spectrums[2] of both the POCSAG (1200 and 2400 bps) and FLEX (6400 and 3200 bps) signals. Nulls occur at DC for POCSAG, whereas important DC components exist in FLEX. The importance of these DC information increases with transmission speed. As a result, the AC coupling method employed in POCSAG receivers[1] is not applicable to FLEX.

To observe the DC offset problem, the error probability of the direct conversion multilevel FSK detector shown in Figure 9 was simulated without zero-crossing

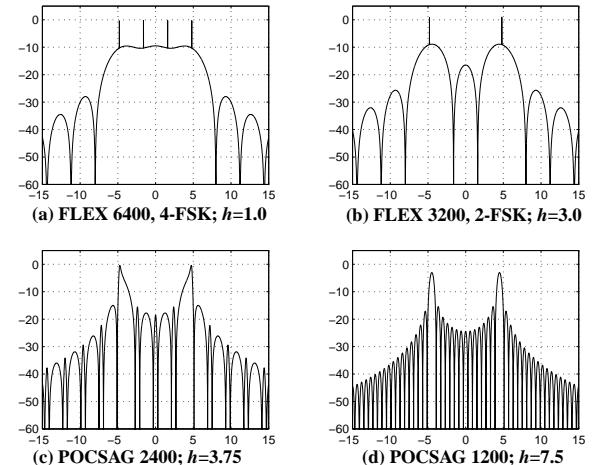


Figure 1. Analytical signal power spectrums of both the FLEX and POCSAG systems at different bit rates. The y-axis is in log-scale. The x-axis is the frequency deviation from the carrier in kHz. h is the modulation index.

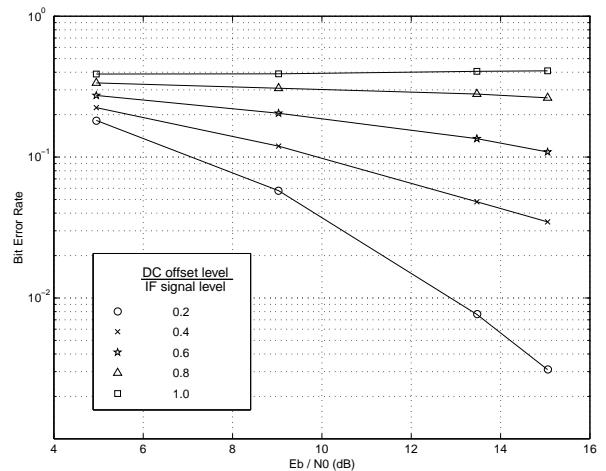


Figure 2. Effect of the DC offset on the BER performance. As the offset level gets strong enough (comparable to the signal level or larger), the detector is eventually out of function.

interpolation. We shall explain the detector and the zero-crossing interpolation technique in later sections. In the

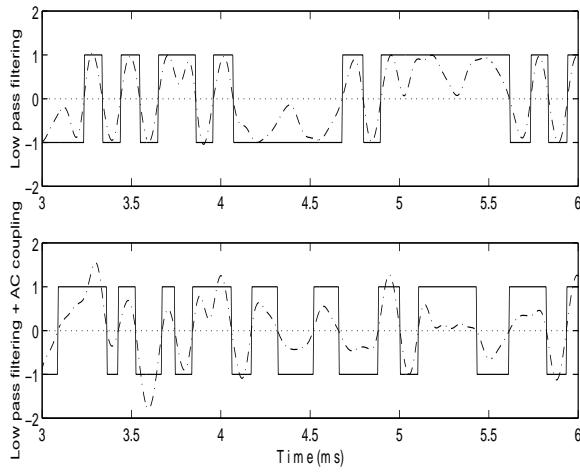


Figure 3. AC coupling introduces significant errors to a low modulation index signal by altering the number and the locations of zero-crossings. The dashed line is the signal waveform and the solid line is its hard-limited output.

simulation, DC offset was injected into the input I and Q waveforms. As can be seen in Figure 2, even a very small DC offset relative to the IF signal strength would degrade the BER sharply. Considering that in today's paging receiver which requires a BER no worse than 3% to keep the success call rate above 80%[3], we can observe that a DC offset as small as half the IF signal is detrimental to the receiver. Unfortunately, the DC offset level can be several hundred times larger than weak signals. Waveforms shown in Figure 3 help explain why AC coupling does not work with FLEX. The top plot shows a low pass filtered signal and its hard limited output which will be used in the following detection stages. The bottom one illustrates the effect of AC coupling to the same signal: the number and positions of zero-crossings change greatly and the information is corrupted.

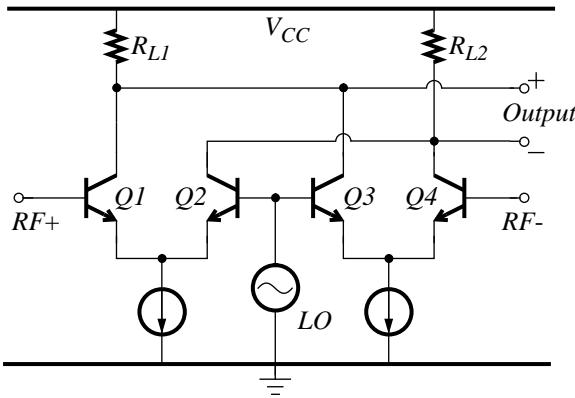


Figure 4. A Balanced 2nd Harmonic Mixer

DC offset compensation methods that have been pro-

posed so far usually require sophisticated DSP-based algorithms. Alternatively, the problem can be greatly simplified using harmonic mixing. Unlike conventional mixers, a harmonic mixer is theoretically free of self-mixing, the main contributor to DC offset. An equivalent input DC offset level of -92dBm has been reported[4] with the balanced harmonic mixer in Figure 4 driven by a -6dBm LO. Ideally, the balanced structure depresses any even order products including the self-mixed DC offset.

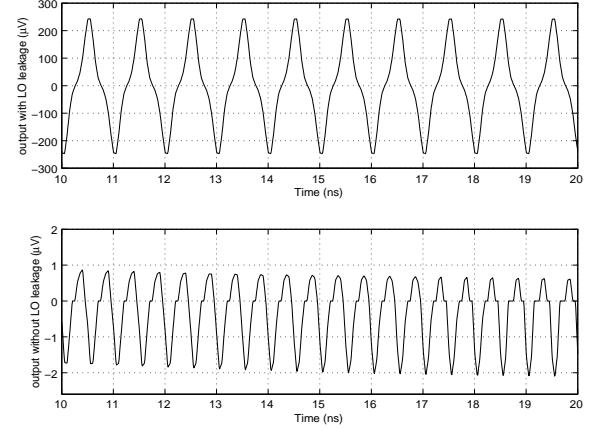


Figure 5. Output waveforms of the harmonic mixer. LO frequency and magnitude are 1.0GHz and 100mV (-10dBm). Those of the RF signal are 2.009GHz and 1.8μV (-105dBm). In the upper plot, 200μV or -64dBm LO leakage at the RF port was assumed (-50dB LO to antenna leakage, -20dB antenna reflection coefficient, 15dB antenna to mixer RF port gain). No LO leakage was considered in the lower one.

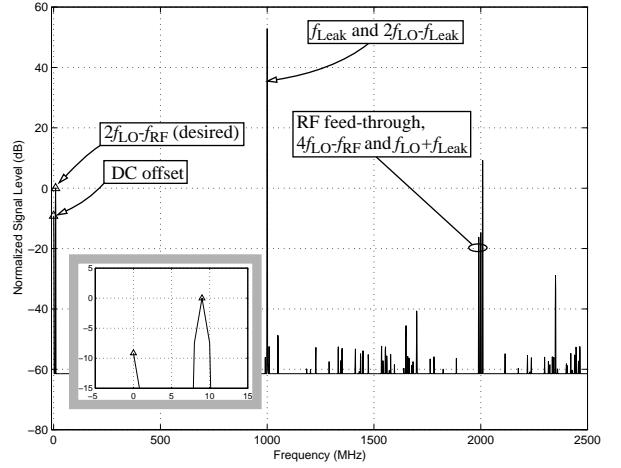


Figure 6. Spectrum analysis of the waveform shown in Figure 5 with LO leakage. The desired component (i.e. the 9MHz signal) is almost 10dB above the DC offset.

An HSPICE simulation based on a 14GHz f_T bipolar transistor model in a BiCMOS process was carried out. With -50dB LO to antenna leakage, -20dB antenna reflec-

tion coefficient and 15dB antenna to mixer RF port amplification, the simulation yielded a DC offset which was almost 10dB below the IF signal when the RF (at the input port of the LNA) and LO signals were -120 and -10 dBm, respectively. Assuming the LO leakage is reflected only by the antenna, these assumptions imply -65dBm LO leakage and -105dBm RF signal at the RF port of the mixer. For the purpose of comparison, we also simulated the ideal condition where the LO signal was isolated perfectly from other ports. Details about the simulation are illustrated in Figure 5, Figure 6 and Figure 7.

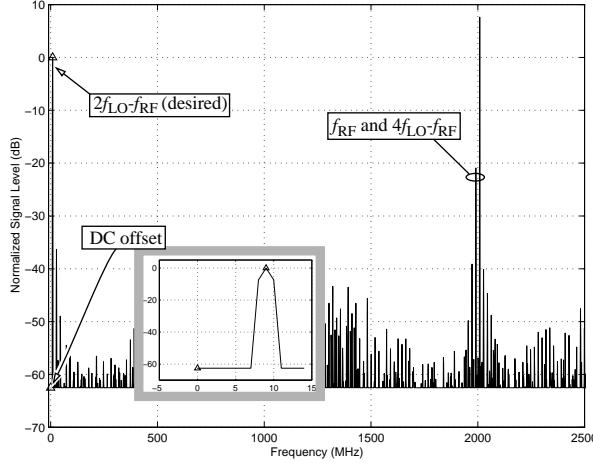


Figure 7. Spectrum analysis of the lower waveform in Figure 5. Without the LO leakage, the DC offset can hardly be observed.

The Demodulation Problem and The Zero-Crossing Interpolation Method

Yet another problem of the direct conversion architecture lies in the design of an effective M-ary FSK demodulator. For high integration and low cost, digital approaches are desired. One such device was conceived by Vance in 1982[5]. In its simplest form, as shown in Figure 8, a D-type flip flop is ready to get the work done. The idea was further developed by Philips[1] and others in their real life applications. Unfortunately, this type of demodulators detect only the phase rotation direction whereas for 4-level FSK signals, the rotation speed has to be captured as well.

It has been demonstrated[6] that the zero-crossing demodulation method is capable of demodulating multi-level low modulation indices FSK signals. The demodulator utilizes a bi-directional counter to monitor both of the phase rotation direction and speed. Its accuracy can be improved by using a technique (termed *zero-crossing interpolation* here) which generates additional zero-crossings for detection. In the demodulation examples of 0.5

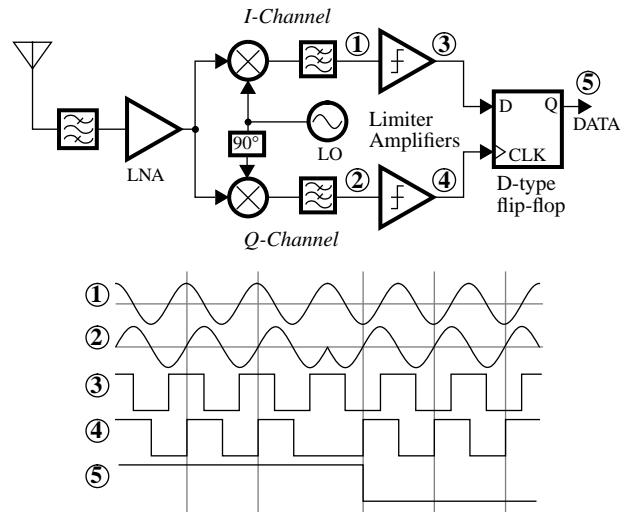


Figure 8. Principle of Vance's direct conversion radio paging receiver.

and 1.5 indices CPFSK signals given in [6], the error probability performances approach those of the LDI (limiter-discriminator with integrator-dump filter) demodulators as more additional zero-crossings are generated. Notice that modulation index of the 6400 bps FLEX signal is 1.0.

In Figure 9 a new architecture is obtained by applying the zero-crossing interpolation technique to the detector proposed by Saitou *et al.* [7]. Simulations are carried out at different interpolation levels (i.e. with different amount of additional zero-crossings). Channel selection is done by two 10th order Bessel low pass filters. Simulation results depicted in Figure 10 show that at the bit error rate of 10^{-2} , the noise immunity is improved by more than 1dB. This improvement relaxes the noise figure requirement of the front-end by the same amount.

Conclusion

In this paper the DC offset problem and the 4-level FSK demodulation problem encountered in the design of direct conversion FLEX paging receivers were discussed. The effectiveness of the harmonic mixing and the zero-interpolation method in solving these problems were also demonstrated. We believe that by applying these two techniques properly and with further improvements, direct conversion can be a solution for FLEX paging receivers.

Acknowledgment

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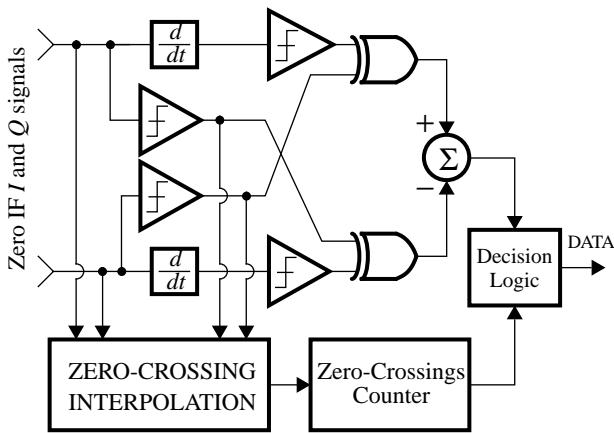


Figure 9. A multilevel FSK detector with zero-crossing interpolation. It can be used in the receiver of Figure 8 by replacing the 2 limiter amplifiers and the D flip flop.

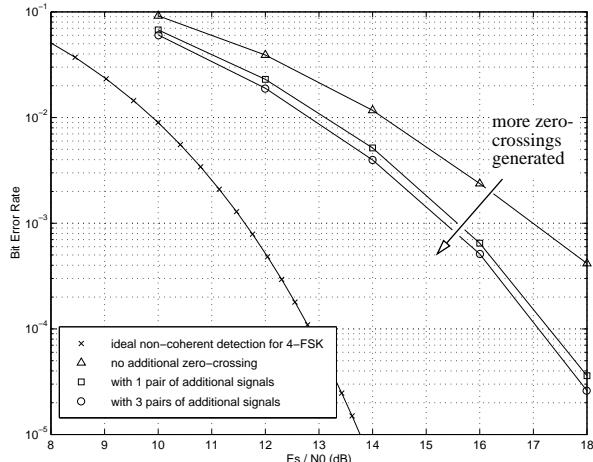


Figure 10. BER performance improved by the zero-crossing generating technique.

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